UČNI NAČRT PREDMETA / COURSE SYLLABUS (leto / year 2017/18)			
Predmet:	Digitalno načrtovanje		
Course title:	Digital design		
Študijski program in stopnja **Study programme and level**	**Študijska smer** **Study field**	**Letnik** **Academic year**	**Semester** **Semester**
Interdisciplinarni univerzitetni študijski program Računalništvo in matematika	ni smeri	3	prvi
Interdisciplinary first cycle academic study programme Computer Science and Mathematics	none	3	first

Vrsta predmeta / Course type	izbirni / elective
Univerzitetna koda predmeta / University course code:	63260

Predavanja **Lectures**	**Seminar** **Seminar**	**Vaje** **Tutorial**	**Klinične vaje** **work**	**Druge oblike študija**	**Samost. delo** **Individ. work**	**ECTS**
45	**10**	**20**			**105**	**6**

Nosilec predmeta / Lecturer:	prof. dr. Patricio Bulić

Jeziki / Languages:	**Predavanja / Lectures:**	slovenski / Slovene
	Vaje / Tutorial:	slovenski / Slovene

Pogoji za vključitev v delo oz. za opravljanje študijskih obveznosti:	**Prerequisites:**
Vpis v letnik študija.	Enrolment in the programme.
Vsebina:	**Content (Syllabus outline):**

Uvod v načrtovanje in testiranje digitalnih sistemov, Jeziki HDL za opis strojne opreme (VHDL, Verilog), napotki za kodiranje, simulacija, sinteza, Tehnologija in pregled programabilnih vezij, Računalniška aritmetika ter načrtovanje in sinteza odločitvenih vezij, Načrtovanje sekvenčnih vezij: sinhrona in asinhrona vezja, pomnilne celice, register, registerski niz, števci, splošni končni avtomat, pomnilnik), Urin signal: sinteza, distribucija, »clock gating«, sinhronizacija, Načrtovanje (mikro)procesorja: podatkovne poti, kontrolna enota, cevovod Načrtovanje sinhronskih komunikacijskih vmesnikov (PS/2, I2C, PCI) Načrtovanje asinhronskih komunikacijskih vmesnikov (USART) Sinteza pomnilnikov RAM in ROM, sinteza dvokanalnih pomnilnikov Sinteza grafičnih vmesnikov Modularna gradnja sistemov: sistem na čipu (SOC, System-on-Chip).	1. Introduction to design and testing of digital systems, 2. Languages for hardware description (VHDL, Verilog, Abel-HDL, …), 3. Technology and survey of programmable logic circuits 4. Computer arithmetics: design and synthesis of decision digital circuits, 5. Design of time dependant synchronous and asynchronous circuits, flip-flops, counters, registers, finite automata, 6. Clock signal, distribution and clock gating, synchronization, 7. Design of microprocessor, data paths, control unit, pipeline, 8. Design of synchronous communication adapters (PS/2, I2C, PCI), 9. Design of asynchronous comm. adapters (USART), 10. Memory synthesis: RAM,ROM, dual-channel 11. Design of simple graphics interfaces 12. Modular system synthesis: system on chip (SOC).

Temeljni literatura in viri / Readings:

Wakerly, John F. Digital design : principles and practices, Upper Saddle River : Pearson/Prentice Hall, 2006,

Enoch Hwang. Digital Logic and Microprocessor Design with VHDL. Thomson/Nelson, 2006.

Richard E. Haskell &, Darrin M. Hanna, Digital Design. 2nd Ed. LBE Books 2012.

Zapiski s predavanj, gradivo za vaje / Lecture notes, exercises

Cilji in kompetence:

Študenta želimo naučiti samostojne uporabe in načrtovanja digitalnih vezij z uporabo sodobnih jezikov HDL in načrtovalskih orodij za simulacijo in sintezo. Pri tem jih opozorimo na specifičnosti le-teh in naučimo upoštevati optimalne pristope. Pri predmetu študentje pridobijo znanje in izkušnje pri načrtovanju in testiranju digitalnih sistemov ter uporabi sodobnih načrtovalskih orodij, razvijejo spretnosti za skupinsko razvojno delo ter poglobijo tehnično znanje.

Objectives and competences:

We instruct students how computer-aided design tools are used to both simulate the VHDL or Verilog design and to synthesize the design to actual hardware. Specific behaviour of HDL tools is emphasized. We present the design of digital circuit using optimal approaches. As part of the course, students develop familiarity and confidence with designing, building and testing digital circuits, including the use of CAD tools, develop team-building skills and enhance technical knowledge through both written assignments and design projects.

Predvideni študijski rezultati:

Znanje in razumevanje:

Razumevanje delovanja brezžičnih omrežij. Poznavanje razlik med različnimi brezžičnimi omrežji ter njihova uporaba.

Uporaba:

Uporaba brezžičnih in mobilnih omrežij pri raznih pogojih uporabe (industrija, hišna omrežja, osebna omrežja, ...).

Refleksija:

Spoznavanje in razumevanje uglašenosti med teorijo in njeno aplikacijo na konkretnih

Intended learning outcomes:

Knowledge and understanding:

104 Introduction to Digital Circuits

202 Computer Systems Architecture

208 Organisation of Computer Systems

Design and implement combinational and sequential logic circuits using VHDL/Verilog, analyze the timing of digital circuits, design and implement state machines, use a complex sequential logic circuit as part of a solution to an open-ended design problem, give oral and written reports on all aspects of a design

primerih s področja brezžičnega prenosa podatkov. Prenosljive spretnosti - niso vezane le na en predmet: Reševanje drugih konceptualno sorodnih problemov (npr. telefonska omrežja 3G in 4G).	project. Application: Design of some complex digital circuits or a part of system on chip (SOC). Reflection: Understanding and the ability to design complex digital systems. Transferable skills: They are not connected only to this particular work. Project report and the design implementation.

Metode poučevanja in učenja:	**Learning and teaching methods:**
Predavanja, laboratorijske vaje na katerih se uporabljajo sodobna orodja za načrtovanje digitalnih sistemov ter vezij FPGA, domače naloge, končni projekt	Lectures, a series of lab assignments using modern CADF tools and FPGAs, homeworks, final project

Načini ocenjevanja:	Delež (v %) / Weight (in %)	**Assessment:**
Način (pisni izpit, ustno izpraševanje, naloge, projekt):		Type (examination, oral, coursework, project):
Sprotno preverjanje (domače naloge, kolokviji in projektno delo)	50%	Continuing (homework, midterm exams, project work)
Končno preverjanje (pisni in ustni izpit)	50%	Final (written and oral exam)
Ocene: 6-10 pozitivno, 1-5 negativno (v skladu s Statutom UL)		Grading: 6-10 pass, 1-5 fail.

Reference nosilca / Lecturer's references:

AVRAMOVIĆ, Aleksej, BABIĆ, Zdenka, RAIČ, Dušan, STRLE, Drago, BULIĆ, Patricio. An approximate logarithmic squaring circuit with error compensation for DSP applications. Microelectronics journal, ISSN 0959-8324. [Print ed.], 2014, vol. 45, iss. 3, str. 263-271. , doi: . [COBISS.SI-ID

10373972]

ČEŠNOVAR, Rok, RISOJEVIĆ, Vladimir, BABIĆ, Zdenka, DOBRAVEC, Tomaž, BULIĆ, Patricio. A GPU implementation of a structural-similarity-based aerial-image classification. The journal of supercomputing, ISSN 0920-8542, Aug. 2013, vol. 65, no. 2, str. 978-996, ilustr. , doi: . [COBISS.SI-ID 9619028]

BULIĆ, Patricio, GUŠTIN, Veselko, ŠONC, Damjan, ŠTRANCAR, Andrej. An FPGA-based integrated environment for computer architecture. Computer applications in engineering education, ISSN 1061-3773. [Print ed.], Mar. 2013, vol. 21, no. 1, str. 26-35, ilustr. , doi: . [COBISS.SI-ID 7696212]

LOTRIČ, Uroš, BULIĆ, Patricio. Applicability of approximate multipliers in hardware neural networks. Neurocomputing, ISSN 0925-2312. [Print ed.], Nov. 2012, vol. 96, str. 57-65, ilustr. [COBISS.SI-ID 9160276]

BABIĆ, Zdenka, AVRAMOVIĆ, Aleksej, BULIĆ, Patricio. An iterative logarithmic multiplier. Microprocessors and microsystems, ISSN 0141-9331. [Print ed.], 2011, vol. 35, no. 1, str. 23-33, ilustr. [COBISS.SI-ID 7837780]